METHOD OF SILICON DEBUG OF CORE BASED SYSTEM-ON-A-CHIP (SOC) AND STRUCTURE OF SOC INCORPORATING SAME

Abstract of the Disclosure

A method of debugging an individual core in core based system-on-a-chip (SOC) ICs with high accuracy and observability, and a structure of SOC incorporating the method. The method includes the steps of building two or more metal layers of a pad frame for each core in an SoC while connecting I/O (input and output) pads on a lower metal layer to a top metal layer, thereby exposing all I/O pads and power pads on a surface of the top metal layer of the pad frame of each core, and applying test vector to each core through the I/O pads on the top metal layer of the core and evaluating response outputs of the core received through the I/O pads on the top metal layer.